



High mobility nMOS substrates: strained-Si, Ge or III-V?

It is clear that for the choice of high hole mobility materials, one is limited to Ge and Ge-rich SiGe alloys. In combination with compressive strain, it has been shown that this will lead to p-type performance which exceeds the best that can be achieved by uniaxially strained silicon. For n-channel materials on the other hand, the last word has not been said yet. There is probably still room for improvement for tensile-strained silicon (on-insulator) material, certainly in combination with process-induced stressors, to maintain a performance enhancement down to the smallest gate lengths. At the same time, the development of n-channel transistors on Ge suffers from some technological challenges like the passivation of the surface and the low activation of the n-type dopants, related with the lower density of states in the conduction band. Recently, however, considerable progress has been made by the implementation of thermal GeO₂, which is shown to be a very good – if not the best – passivation layer, giving rise to ever increasing electron mobility. At the moment, it is not clear whether the full potential of a two times improvement compared with silicon is in reach or not, since this will also require a better activation of the source/drain regions or even the use of Schottky barrier contacts.

While III-V alloys have a clear low-field mobility advantage compared with silicon and germanium, the surface passivation and dopant activation issues appear to be even more severe than in germanium. This explains why besides traditional MIS schemes alternative architectures are being explored.

The aim of the visionary workshop would be to review the state-of-the-art of the main contenders for high-mobility n-MOS materials, to point out the issues and opportunities and how these obstacles can be overcome. Confronting the different options should stimulate discussions and point out the most promising route(s) for the industrial implementation of future high-mobility CMOS.

Timing: 14.00-18.00, 17th March 2010

Venue: Room 408, Rankine Building, University of Glasgow

Final Program

14.00-14.10: Opening address - E. Simoen

14.10-14.50: A. Asenov, University of Glasgow, UK: Modeling perspective of future n-channel high-mobility transistors

14.50-15.30: A. Dimoulas, Demokritos, Greece: The DUALLOGIC route to high-mobility n-channel devices

15.30-15.50: Coffee Break

15.50-16.30: M. Meuris, IMEC, Belgium: The challenges of integrating III-V nMOS in next generation CMOS circuits

16.30-17.10: C. Le Royer, CEA-LETI, Minatec, France: Opportunities and challenges of the GeOI platform for future CMOS

17.10-17.55: Panel Discussion

17.55: Closing Address