

# ULIS CONFERENCE PROGRAM

Monday, 5th of March

## TUTORIALS

See Tutorial program

## WELCOME RECEPTION

6 pm

Tuesday 6th of March

## CONFERENCE

8:45 – 9:00 **Opening**

### Invited paper by Pr Shinichi Takagi, Tokyo University

9:00 – 9h:45 *“High Mobility CMOS Technologies using III-V/Ge Channels on Si platform”*

Chair: S. Deleonibus, CEA-LETI

9:45 – 10:45 **SESSION 1 : Channel and gate stack engineering**  
Chairs: G. Doornbos, TSMC, T. Ernst, CEA-LETI

9:45 – 10:05 **Mobility and Strain Effects for <100> and <110> oriented Silicon and SiGe Transistor Channels**

S. Flachowsky<sup>1</sup>, T. Herrmann<sup>1</sup>, J. Höntschel<sup>1</sup>, R. Illgen<sup>1</sup>, Shiang Yang Ong<sup>1</sup>, M. Wiatr<sup>1</sup>, T. Baldau<sup>1</sup>, W. Klix<sup>2</sup>, R. Stenzel<sup>2</sup>

1) GLOBALFOUNDRIES Dresden Module One LLC & Co. KG, Wilschdorfer Landstraße 101, 01109 Dresden, Germany

2) Department of Electrical Engineering, University of Applied Sciences Dresden, Friedrich-List-Platz 1, 01069 Dresden, Germany

10:05 – 10:25 **On the Understanding of the Effects of High Pressure Deuterium and Hydrogen Final Anneal**

C. Diouf<sup>1, 2</sup>, A. Cros<sup>1</sup>, S. Renard<sup>1</sup>, X. Federspiel<sup>1</sup>, M. Rafik<sup>1</sup>, A. Bianchi<sup>1</sup>, J. Rosa<sup>1</sup>, G. Ghibaudo<sup>2</sup>

1) STMICROELECTRONICS, 850 rue Jean Monnet, BP 16, 38926, Crolles, France

2) IMEP-LAHC, MINATEC/INPG, BP 257, 38016 Grenoble, France

10:25 – 10:45 **In depth analysis of dopant effect on high-K metal gate effective work function**

C.Leroux<sup>1</sup>, S.Baudot<sup>1,2</sup>, M.Charbonnier<sup>1</sup>, A.Van Deer Geest<sup>1</sup>, P.Caubet<sup>2</sup>, A.Toffoli<sup>1</sup>, Ph.Blaise<sup>1</sup>, G.Ghibaudo<sup>3</sup>, F.Martin<sup>1</sup>, G.Reibold<sup>1</sup>

1) CEA, LETI, MINATEC Campus, 17 rue des Martyrs, F-38054 Grenoble Cedex 9, France.

2) ST-Microelectronics, 850, rue Jean Monnet, 38926, Crolles cedex, France.

3) IMEP, MINATEC 3, parvis Louis Néel, BP 257, 38016, Grenoble cedex, France.

10:45 – 11:15 **COFFEE BREAK**

11:15 – 12:35 **SESSION 2 : Graphene and III-V MOSFETs**  
Chairs: M Lemme, KTH, C. Fiegna, ARCES-DEIS

11:15 – 11:35 **Graphene-Based Embedded-Oxide-Trap Memory (gEOTM) for Flexible Electronics Application**

S.M. Kim<sup>1</sup>, S. Lee<sup>1, 2</sup>, E. B. Song<sup>1</sup>, S. Seo<sup>3</sup>, D. H. Seo<sup>4</sup> and K. L. Wang<sup>1</sup>

1) Department of Electrical Engineering, University of California, 420 Westwood Plaza, Los Angeles, CA 90095 USA

2) Quantum-functional Semiconductor Research Center, Dongguk University – Seoul, Seoul 100-715, Korea

3) Department of Physics, Sejong University, 98 Gunja-Dong, Gwangjin-Gu, Seoul, 143-747, Korea

4) SAIT, Samsung Electronics Co. Ltd. San 24, Giheung-Gu, Yongin-City, Gyeonggi-Do, 446-711, Korea

11:35 – 11:55 **Strain Engineering in Suspended Graphene Devices for Pressure Sensor Applications**

A.D. Smith, S. Vaziri, A. Delin, M. Östling, M.C. Lemme

KTH Royal Institute of Technology, Integrated Devices and Circuits, Stockholm, Sweden

11:55 – 12:15 **Origins of the Short Channel Effects Increase in III-V nMOSFET Technologies**

T. Dutta<sup>1</sup>, Q. Raffhay<sup>1</sup>, R. Clerc<sup>1</sup>, J. Lacord<sup>2</sup>, S. Monfray<sup>2</sup>, G. Pananakakis<sup>1</sup>, F. Boeuf<sup>2</sup> and G. Ghibaudo<sup>1</sup>

1) IMEP-LAHC, MINATEC Campus, 3 parvis Louis Neel, 38016 Grenoble, France

2) STMicroelectronics, 850, rue J. Monnet, BP. 16, 38921 Crolles, France.

12:15 – 12:35 **Study of Interface and Oxide Defects in High-k/In<sub>0.53</sub>Ga<sub>0.47</sub>As n-MOSFETs**

V. Djara<sup>1</sup>, Student Member, IEEE, K. Cherkaoui<sup>1</sup>, M. Schmidt<sup>1</sup>, Y. Y. Gomeniuk<sup>2</sup>, É. O'Connor<sup>1</sup> I. M. Povey<sup>1</sup>, D. O'Connell<sup>1</sup>, S. Monaghan<sup>1</sup>, M. E. Pemble<sup>1</sup> and P. K. Hurley<sup>1</sup>

1) Tyndall National Institute, University College Cork, Cork, Ireland

2) Lashkaryov Institute of Semiconductor Physics, National Academy of Sciences of Ukraine, Kiev, Ukraine

12:35 – 14:00 **LUNCH**

**Invited paper by Dr. Wilfried Haensch, IBM****14:00 – 14:45***“Exploration of new device concepts for 15 nm node and beyond”*

M. Haond, ST Microelectronics

**14:45 – 16:05****SESSION 3 : Silicon nanowires**

Chairs: F. Balestra, IMEP, N. Collaert, IMEC, S. Roy, University of Glasgow

14:45 – 15:05

**Scaling of High- $\kappa$ /Metal-Gate Trigate SOI Nanowire Transistors down to 10nm width**R. Coquand<sup>1,2,3</sup>, S. Barraud<sup>1</sup>, M. Cassé<sup>1</sup>, P. Leroux<sup>1,4</sup>, C. Vizioz<sup>1</sup>, C. Comboroure<sup>2</sup>, P. Perreau<sup>1</sup>, E. Ernst<sup>1</sup>, M.-P. Samson<sup>2</sup>, V. Maffini-Alvaro<sup>1</sup>, C. Tabone<sup>1</sup>, S. Barnola<sup>1</sup>, D. Munteanu<sup>4</sup>, G.Ghibaud<sup>3</sup>, S. Monfray<sup>2</sup>, F. Boeuf<sup>2</sup>, T. Poiroux<sup>1</sup>

1)CEA-LETI, MINATEC, 17 avenue des Martyrs 38054 Grenoble Cedex 9, France

2) STMicroelectronics, 850 rue J. Monnet, 38926 Crolles Cedex, France

3) IMEP-LAHC, 3 parvis Louis Néel, BP257, 38016 Grenoble Cedex 1, France

4) IM2NP - UMR CNRS 4262, Bât. IRPHE, 49, rue Joliot Curie, BP 146, 13384 Marseille Cedex 13, France

15:05 – 15:25

**Mechanisms of High Hole Mobility in (100) Nanowire pMOSFETs with Width of Less Than 10nm**

H. Nomura, Ryota Suzuki, T. Kutsuki, T. Saraya, and T. Hiramoto

Institute of Industrial Science, University of Tokyo, 4-6-1, Komaba, Meguro, Tokyo, 153-8505, Japan

15:25 – 15:45

**Nanowire and Planar UTB SOI Schottky Barrier MOSFETs with Dopant Segregation**L. Knoll<sup>1</sup>, A. Schäfer<sup>1</sup>, S. Trellenkamp<sup>1</sup>, K.K. Bourdelle<sup>2</sup>, Q.T. Zhao<sup>1</sup> and S. Manti<sup>1</sup>

1) Peter-Grünberg-Institut (PGI 9-IT) and JARA-FIT Forschungszentrum Jülich, Germany

2) SOITEC, Parc Technologique des Fontaines, 38190 Bernin, France.

15:45 – 16:05

**Orientalional and strain dependence of the mobility in silicon nanowires**Y. M. Niquet<sup>1</sup>, C. Delerue<sup>2</sup> and D. Rideau<sup>3</sup>

1) L Sim, SP2M, UMR-E CEA/UJF-Grenoble 1, INAC, Grenoble, France

2) IEMN - Dept. ISEN, Lille, France

3) STMicroelectronics, Crolles, France

16:05 – 16:25

**Strained Silicon Nanowire Array MOSFETs with High- $\kappa$ /Metal Gate Stack**S. Richter<sup>1</sup>, S. Trellenkamp<sup>1</sup>, M. Schmidt<sup>1</sup>, A. Schäfer<sup>1</sup>, K. K. Bourdelle<sup>2</sup>, Q. T. Zhao<sup>1</sup>, S. Manti<sup>1</sup>

1) Peter-Grünberg-Institut (PGI 9-IT), JARA-FIT, Forschungszentrum Jülich, 52425 Jülich, Germany

2) SOITEC, Parc Technologique des Fontaines, 38190 Bernin, France

**16:25 – 18:30****POSTER SESSION**

P1

**RF passives on deep level impurity compensated Cz-Si substrates**

A. Abuelgasim, K. Mallik, P. Ashburn, C.H. de Groot

University of Southampton

P2

**Transport behaviors of graphene 2D field-effect transistors on boron nitride substrate**

A. Alarcón, V. Hung Nguyen, J. Saint-Martin, A. Bournel and P. Dollfus

Université Paris Sud

P3

**Comparison between low and high read bias in FB-RAM on UTBOX FDSOI devices**

L. Mendez Almeida, M. Aoulaiche, K. R. A. Sasaki, T. Nicoletti, M. G. C. de Andrade, N. Collaert, E.

Simoen, C. Claeys, J. A. Martino and M. Jurczak

University of São Paulo

imec KULeuven

P4

**La<sub>0.7</sub>Sr<sub>0.3</sub>MnO<sub>3</sub> thin films on Silicon substrates as uncooled thermal detector**A. Aryan<sup>1</sup>, Jean-Marc Routoure<sup>1</sup>, Bruno Guillet<sup>1</sup>, Pierre Langlois<sup>1</sup>, Cédric Fur<sup>1</sup>, Julien Gasnier<sup>1</sup>,Carolina Adamo<sup>2</sup>, Darrell G. Schlom<sup>2,3</sup> Laurence Méchin<sup>1</sup>

1) Université de Caen Basse-Normandie, UMR 6072 GREYC, F-14032 Caen, France.

2) Department of Materials Science and Engineering, Cornell University, Ithaca, New York 14853

3) Kavli Institute at Cornell for Nanoscale Science, Ithaca, New York 14853, USA

P5

**Energy Capability of LDMOS as a Function of Ambient Temperature**

A. Basavalingappa, Anumeha, Gene Sheu

Asia University, Taiwan

P6

**Low-Frequency Noise Behaviour of Bulk and DTMOS Triple-Gate Devices under 60 MeV Proton Irradiation**

M-G. Caño de Andrade, J.-A. Martino, M. Aoulaiche, N. Collaert, E. Simoen and C. Claeys

University of Sao Paulo imec E. E. Dept., KU Leuven

P7

**Temperature Dependence of Compact Analytical Modeling of Gate Tunneling Current in Double Gate MOSFETs**G. Darbandy<sup>1</sup>, I. Garduño<sup>2</sup>, A. Cerdeira<sup>2</sup> and B. Ifiguez<sup>1</sup>

1) Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili, Spain

2) Department of Electrical Engineering, Section of Solid-State Electronics, CINVESTAV-IPN, Mexico D.F., Mexico

P8

**Single Electron CMOS-Like One Bit Full Adder**D. Griveau<sup>1</sup>, S. Ecoffey<sup>1</sup>, R. M. Parekh<sup>1</sup>, M. A. Bounouar<sup>1,2</sup>, F. Calmon<sup>2</sup>, J. Beauvais<sup>1</sup>, D. Drouin<sup>1</sup>

(1) 3IT, Université de Sherbrooke, Sherbrooke, QC, Canada;

(2) Lyon Institute of Nanotechnology, University of Lyon, INSA-Lyon, F-69621 Villeurbanne Cedex, France

- P9 **2D Analytical Potential Modeling of Junctionless DG MOSFETs in Subthreshold Region Including Proposal for Calculating the Threshold Voltage**  
T. Holtij, Mike Schwarz, A. Kloes and B. Iníguez  
Technische Hochschule Mittelhessen Uni. Rovira I Virgili
- P10 **Designing a new structure for controlling current gain in BJT-transistors**  
S. Ebrahim Hosseini, H. Goodarzi Dehrizi  
Sabzevar Tarbiat Moallem University, Sabzevar, Iran
- P11 **Experimental Investigation on Direction Dependence of Si (100) and Si (110) Hole Mobility in Ultra-Thin Body pFETs**  
T. Kutsuki, K. Shimizu, H. Nomura, T. Saraya, and T. Hiramoto  
University of Tokyo
- P12 **Charge Granularity in Single Electron Transistors with Polysilicon Gates**  
D. Kotekar-Patil, S. Jauerneck, M. Ruoff, D. Wharam, D. Kern, X. Jehl, R. Wacquez, M. Sanquer  
Institute for Applied Physics, University of Tübingen, Germany SPSMS, UMR-E  
CEA/UJF-Grenoble 1, INAC, and CEA/LETI-MINATEC Grenoble F-38054, France
- P13 **Theory of graphene-field effect transistors**  
D. Jiménez and O. Moldovan  
Departament d'Enginyeria Electrònica; Escola d'Enginyeria; U
- P14 **Impact of bulk defects in Hydrogenated amorphous Si layers on performance of high efficiency HeteroJunctions Solar Cells assessed by 2D modelling**  
R. Lachaume<sup>1</sup>, J. Coignus<sup>2</sup>, X. Garros<sup>1</sup>, P. Scheiblin<sup>1</sup>, D. Muñoz<sup>2</sup> and G. Reibold<sup>1</sup>  
1) CEA, LETI, MINATEC Campus, 17 rue des Martyrs, F-38054 GRENOBLE Cedex 9  
2) CEA, INES RDI, 50 avenue du Lac Léman - Savoie Technolac - BP332, F-73377 Le-Bourget-du-Lac
- P15 **Nanometric Thickness Optimization of the Base SiGeC HBT Dedicated to the Radiofrequency**  
M. Lakhdera<sup>1</sup>, S. Latreche<sup>1</sup>, M. R. Beghoul<sup>1</sup>, and C. Gontrand<sup>2</sup>  
1) Laboratoire Hyperfréquence & Semi-conducteur (LHS), Département d'Electronique Université Mentouri, Constantine, 25000, ALGERIA  
2) INL, Institut des Nanotechnologies de Lyon, INSA- Lyon, CNRS France.
- P16 **Quantum Point Contact model of filamentary conduction in resistive switching memories**  
X. Lian, S. Long, C. Cagli, J. Buckley, E. Miranda, M. Liu, J. Suñé  
1)Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Spain  
2)CEA-LETI, MINATEC, Grenoble, France  
3)Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China.
- P17 **In situ SiO<sub>x</sub> interfacial layer formation for scaled ALD high-k/metal gate stacks**  
E. Dentoni Litta, P.-E. Hellström, C. Henkel, M. Östling  
KTH Royal Institute of Technology, School of ICT, Sweden
- P18 **On Extraction of Self-Heating Features in UTBB SOI MOSFETs**  
S. Makovejev, S. Olsen, F. Andrieu, T. Poiroux, O. Faynot, D. Flandre, J.-P. Raskin, V. Kilchytska  
Newcastle University  
CEA-LETI, MINATEC, Grenoble, France  
Université catholique de Louvain
- P19 **Device Scaling Model for Bulk FinFETs**  
A. Medury, K. Mercha, R. Ritzenthaler, A. De Keersgieter, T. Chiarella, N. Bhat and K.N Bhat  
CENSE, IISc, Bangalore, India.  
IMEC, Leuven, Belgium
- P20 **Assessment of NBTI in Presence of Self-heating in High-k SOI FinFETs**  
U. Monga, S. Khandelwal, J. Aghassi, J. Sedlmeir, T. A. Fjeldly  
Intel Mobile Communications GmbH, Munich,  
NTNU, Norway
- P21 **Capacitance and Resistance Extraction of Through-Silicon Via (TSV) in 3-D Technology**  
M. Alidusti, M. Monavarian, R. Sarvari  
Dept. of Electrical Engineering, Sharif University of Technology
- P22 **Very large piezoresistance in Si<sub>1-x</sub>Ge<sub>x</sub> alloys**  
F. Murphy-Armando and S. Fahy  
Tyndall National Institute, University College Cork
- P23 **The Impact of Gate Length Scaling on UTBOX FDSOI Devices: the Digital/Analog Performance of Extension-less Structures**  
T. Nicoletti S. Santos L. Almeida J. A. Martino M. Aoulache A. Veloso M. Jurczak E. Simoen C. Claeys  
LSI/PSI/EPUSP - University of Sao Paulo imec E.E. Dept., KU Leuven
- P24 **Intrinsic Gate Delay and Energy-Delay Product in Junctionless Nanowire Transistors**  
P. Razavi, I. Ferain, S. Das, R. Yu, N. D. Akhavan, J.-P. Colinge  
Tyndall National Institute, University College Cork

- Realization of both a single electron transistor and a field effect transistor with an underlapped FDSOI MOSFET geometry**  
P25 B. Roche, B. Voisin, R. Wacquez, M. Sanquer, M. Vinet, V. Deshpande, B. Previtali  
CEA, INAC, SPSMS, 17 rue des Martyrs, F-38054 GRENOBLE Cedex 9  
CEA, LETI, MINATEC Campus, 17 rue des Martyrs, F-38054 GRENOBLE Cedex 9
- Explicit Model for Tunneling and Thermionic Current in Schottky Barrier Double-Gate MOSFETS**  
P26 M. Schwarz (1,2), T. Holtij (1,2), A. Kloes (1), and B. Iñiguez (2)  
1) THM, Giessen, Germany  
2) URV, Tarragona, Spain
- Design and Analysis of New sub-threshold DTMOS SRAM Cell Structure**  
P27 S. Soleimani-Amiri, A. Afzali-Kusha  
School of Electrical and Computer Engineering of Tehran, Iran Tehran, Iran
- Accurate Modeling of SOI Multi-Gate FETs and Their Transient Response to Radiation**  
P28 M. Turowski<sup>1</sup>, A. Raman<sup>1</sup>, and W. Xiong<sup>2</sup>  
1) CFD Research Corporation (CFDRC), USA;  
2) SEMATECH, USA
- TAMTAMS: a flexible and open tool for UDSM process-to-system design space exploration**  
P29 M. Vacca, M. Graziano, D. Demarchi and G. Piccinini  
Department of Electronics and Telecommunications, Politecnico di Torino, Torino, Italy
- Top-down Process of Germanium Nanowires using EBL Exposure of Hydrogen Silsesquioxane Resist**  
P30 R. Yu\*, S. Das, R. Hobbs, Y. Georgiev, I. Ferain, P. Razavi, N. Dehdashti Akhavan, C. A. Colinge and J.-P. Colinge  
Tyndall National Institute

**19:00 – 23:00 BEST PAPER AWARD & GALA DINNER**

**Wednesday 7th of March**

**8:40 – 9h:25**

**Invited paper by Dr Eberle Wolfgang, IMEC**  
*"Bio-nano-electronics interfacing at the single-cell level"*  
Chair: Y. Ponomarev, NXP

**9:25 – 10:45**

**SESSION 4 : Disruptive and More than Moore devices**  
Chairs: L. Selmi, University of Udine , S. Mantl, Juelich

9:25 – 9:45

**Efficient DC and AC simulation of nanoelectrode-nanoparticle interactions in capacitive biosensors**

F. Pittino<sup>1</sup>, F. Widdershoven<sup>2</sup>, L. Selmi<sup>1</sup>  
1) DIEGM, Università degli Studi di Udine, Udine, Italy, fedepittino@gmail.com  
2) NXP Semiconductors, Leuven, Belgium

9:45 – 10:05

**Numerical Simulation and Modeling of Thermal Transient in Silicon Power Devices**

P. Magnone<sup>1</sup>, C. Fiegna<sup>1</sup>, G. Greco<sup>2</sup>, G. Bazzano<sup>2</sup>, S. Rinaudo<sup>2</sup>, E. Sangiorgi<sup>1</sup>  
1) ARCES, University of Bologna and IUNET, I-47521 Cesena (FC), Italy  
2) STMicroelectronics, I-95121 Catania, Italy

10:05 – 10:25

**On the Use of Nanoelectronic Logic Cells Based on Metallic Single Electron Transistors**

M. A. Bounouar<sup>1,2</sup>, A. Beaumont<sup>2</sup>, F. Calmon<sup>2</sup>, D. Drouin<sup>1</sup>  
1) 3IT-CRN2, Dept. of Electrical and Computer Engineering, University of Sherbrooke, Sherbrooke, QC, Canada  
2) Lyon Institute of Nanotechnology, University of Lyon, INSA-Lyon, F-69621 Villeurbanne Cedex, France

10:25 – 10:45

**Characteristics Control of Single Electron Transistor with Floating Gate by Charge Pump Circuit**

M. Nozue, R. Suzuki, H. Nomura, T. Saraya, and T. Hiramoto  
Institute of Industrial Science, University of Tokyo, 4-6-1, Komaba, Meguro-ku, Tokyo, 153-8505, Japan

**10:45 – 11:15 COFFEE BREAK**

**11:15 – 12:35** | **SESSION 5 : Advanced FDSOI CMOS**  
Chairs: G. Ghibaudo, IMEP, J. Hoentschel, Global Foundries

**11:15 – 11:35** | **Impact of local back biasing on performance in hybrid FDSOI/Bulk high-k/Metal gate Low Power (LP) technology**  
C.Fenouillet-Beranger<sup>2,1</sup>, P. Perreau<sup>2,1</sup>, T. Benoist<sup>1,2,3</sup>, C. Richier<sup>1</sup>, S. Haendler<sup>1</sup>, J. Pradelle<sup>2</sup>, J. Bustos<sup>2</sup>, P. Brun<sup>2,1</sup>, L. Tosti<sup>2</sup>, O. Weber<sup>2</sup>, F. Andrieu<sup>2</sup>, B. Orlando<sup>1</sup>, D. Pellissier-Tanon<sup>1</sup>, F. Abbate<sup>1</sup>, C. Richard<sup>1</sup>, R. Beneyton<sup>1</sup>, M. Gregoire<sup>1</sup>, J. Ducote<sup>1</sup>, P. Gouraud<sup>1</sup>, A. Margain<sup>1</sup>, C. Borowiak<sup>1</sup>, R. Bianchini<sup>1</sup>, N. Planes<sup>1</sup>, E. Gourvest<sup>1</sup>, K.K. Bourdelle<sup>4</sup>, B.Y. Nguyen<sup>4</sup>, T. Poiroux<sup>2</sup>, T.Skotnicki<sup>1</sup>, O. Faynot<sup>2</sup>, F. Boeuf<sup>1</sup>  
1) STMicroelectronics, 850, rue J.Monnet, BP. 16, 38921 Crolles, France.  
2) CEA-LETI MINATEC, 17 rue des Martyrs, 38054 Grenoble, Cedex 9, France  
3) IMEP, MINATEC 3 Parvis Louis Neel, 38016 Grenoble, Cedex 1, France,  
4) SOITEC, Parc Technologique des Fontaines, Bernin, 38926 Crolles, France

**11:35 – 11:55** | **FDSOI devices: a solution to achieve low junction leakage with low temperature processes ( $\leq 650^{\circ}\text{C}$ )**  
B. Sklénard<sup>1,2,3</sup>, C. Xu<sup>2</sup>, P. Batude<sup>2</sup>, B. Previtali<sup>2</sup>, C. Tabone<sup>2</sup>, Q. Rafhay<sup>3</sup>, B. Colombeau<sup>5</sup>, F.-A. Khaja<sup>5</sup>, I. Martín-Bragado<sup>4</sup>, J. Berthoz<sup>2</sup>, F. Allain<sup>2</sup>, A. Toffoli<sup>2</sup>, R. Kies<sup>2</sup>, M.-A. Jaud<sup>2</sup>, P. Rivallin<sup>2</sup>, S. Cristoloveanu<sup>3</sup>, C. Tavernier<sup>1</sup>, O. Faynot<sup>2</sup>, T. Poiroux<sup>2</sup>  
1) STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles  
2) CEA, LETI, MINATEC Campus, 17 rue des Martyrs, F-38054 Grenoble Cedex 9  
3) IMEP-LAHC, 3 parvis Louis Néel, F-38016 Grenoble  
4) IMDEA Materials Institute, Calle Profesor Aranguren s/n., 28040 Madrid, Spain  
5) Varian Semiconductor Equipment Associates, 35 Dory Road, Gloucester, MA 01930, USA

**11:55 – 12:15** | **Comparison between  $\langle 100 \rangle$  and  $\langle 110 \rangle$  oriented channels in highly strained FDSOI nMOSFETs**  
S. Morvan<sup>1</sup>, F. Andrieu<sup>1</sup>, M. Cassé<sup>1</sup>, P. Nguyen<sup>3</sup>, O. Weber<sup>1</sup>, P. Perreau<sup>1</sup>, C. Tabone<sup>1</sup>, F. Allain<sup>1</sup>, A. Toffoli<sup>1</sup>, G. Ghibaudo<sup>2</sup> and T. Poiroux<sup>1</sup>  
1) CEA-LETI, MINATEC campus, 38054 Grenoble Cedex 9, France  
2) IMEP-LAHC, MINATEC, INP Grenoble, BP 257, 38016 Grenoble, France  
3) SOITEC, Parc Technologique des Fontaines, 38190 Bernin, France

**12:15 – 12:35** | **Impact of substrate orientation on Ultra Thin BOX Fully Depleted SOI electrical performances**  
I. Ben Akkez<sup>1,3</sup>, C.Fenouillet-Beranger<sup>2,1</sup>, A. Cros<sup>1</sup>, P. Perreau<sup>2,1</sup>, S.Haendler<sup>1</sup>, O. Weber<sup>2</sup>, F.Andrieu<sup>2</sup>, D. Pellissier-Tanon<sup>1</sup>, F. Abbate<sup>1</sup>, C. Richard<sup>1</sup>, R. Beneyton<sup>1</sup>, P. Gouraud<sup>1</sup>, A. Margain<sup>1</sup>, C. Borowiak<sup>1</sup>, E. Gourvest<sup>1</sup>, K.K. Bourdelle<sup>4</sup>, B.Y. Nguyen<sup>4</sup>, T. Poiroux<sup>2</sup>, T.Skotnicki<sup>1</sup>, O. Faynot<sup>2</sup>, F. Balestra<sup>3</sup>, G. Ghibaudo<sup>3</sup>, F. Boeuf<sup>1</sup>.  
1) STMicroelectronics, 850, rue J.Monnet, BP. 16, 38921 Crolles, France.  
2) CEA-LETI MINATEC, 17 rue des Martyrs, 38054 Grenoble, Cedex 9, France ;  
3) IMEP-LAHC, MINATEC 3 Parvis Louis Néel, 38016 Grenoble, Cedex 1, France,  
4) SOITEC, Parc Technologique des Fontaines, Bernin, 38926 Crolles, France

**12:35 – 14:00** | **LUNCH**

**Invited paper by Pr Yusuf Leblebici, EPFL**

**14:00 – 14:45** | *"Nanometer-scale system design challenges: bridging the gap from devices to architectures."*  
Chair: E. Sangiorgi

**14:45 – 15:45** | **SESSION 6 : Tunnel FET**  
Chairs: S. Monfray, ST Microelectronics, Q. Rafhay, IMEP

**14:45 – 15:05** | **Investigation of localized versus uniform strain as a performance booster in InAs Tunnel-FETs**  
F. Conzatti<sup>1</sup>, M.G. Pala<sup>2</sup>, D. Esseni<sup>1</sup>, E. Bano<sup>2</sup> and L. Selmi<sup>1</sup>  
1) DIEGM, Via delle Scienze 208, 33100 Udine, Italy  
2) IMEP-LAHC, Grenoble INP, MINATEC, 3 Parvis Louis Néel, 38016 Grenoble, France

**15:05 – 15:25** | **Multi-Subband Semi-classical Simulation of n-type Tunnel-FETs**  
A. Revelant, P. Palestri and L. Selmi  
DIEGM, University of Udine- IU.NET, Via delle Scienze 208, 33100, Udine, Italy,

**15:25 – 15:45** | **Si/SiGe Hetero-Structure Tunneling Field Effect Transistors with In-Situ Doped SiGe Source**  
M. Schmidt<sup>1</sup>, L. Knoll<sup>1</sup>, S. Richter<sup>1</sup>, A. Schäfer<sup>1</sup>, J.-M. Hartmann<sup>2</sup>, Q. T. Zhao<sup>1</sup>, S. Manti<sup>1</sup>  
1) Peter Grünberg Institute 9 (PGI 9-IT), JARA-FIT, Forschungszentrum Jülich, 52425 Jülich, Germany  
2) CEA-LETI, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble, France

**15:45 – 16:05** | **COFFEE BREAK**

**16:05 – 17:05** | **SESSION 7 : Advanced memory concepts and models**

Chairs: J. Sune, UA Barcelona

16:05 – 16:25 | **Downscaling Ferroelectric Field Effect Transistors by using ferroelectric Si-doped HfO<sub>2</sub>**

D. Martin<sup>1</sup>, E. Yurchuk<sup>1</sup>, S. Müller<sup>1</sup>, J. Müller<sup>2</sup>, J. Paul<sup>2</sup>, J. Sundquist<sup>2</sup>, S. Slesazek<sup>1</sup>, T. Schloesser<sup>3</sup>, R. van Bentum<sup>3</sup>, M. Trentzsch<sup>3</sup>, U. Schroeder<sup>1</sup>, and T. Mikojajick<sup>1,4</sup>

1) NamLab GmbH, 01187 Dresden, Germany

2) Fraunhofer Center Nanoelectronic Technologies(CNT), 01099 Dresden, Germany

3) GLOBALFOUNDRIES Dresden Module One LLC & Co. KG, 01109 Dresden, Germany

4) Chair of Nanoelectronic Materials, Technische Universität Dresden, 01062 Dresden, Germany

16:25 – 16:45 | **Surface potential compact model for embedded flash devices oriented to IC memory design**

D. Garetto<sup>1,2</sup>, D. Rideau<sup>2</sup>, F. Gilibert<sup>2</sup>, A. Schmid<sup>2</sup>, H. Jaouen<sup>2</sup>, and Y. Leblebici<sup>2</sup>

1) IBM Systems and Technology Group - 850, rue Jean Monnet, Crolles, France -

2) Ecole Polytechnique Fédérale de Lausanne - Lausanne, Switzerland

16:45 – 17:05 | **Compact (Wg/Lg=80/85nm) FDSOI 1T-DRAM programmed by Meta Stable Dip**

K. Romanjek, F. Andrieu, J. Cluzel, L. Brevard, P. Perreau, C. Tabone, G. Guegan and T. Poiroux  
CEA-Leti, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France

**17:05 – 17:15** | **Closing**

